What is claimed is:

1. A demodulator circuit for emulating the down conversion of an input signal x(t) with a local oscillator (LO) signal, said demodulator circuit comprising:

a first mixer for receiving said input signal x(t), and mixing said input signal x(t) with a multi-tonal mixing signal φ1, to generate an output signal φ1 x(t);

a second mixer for receiving said signal φ1 x(t) as an input, and mixing said signal φ1 x(t) with a mono-tonal mixing signal φ2, to generate an output signal φ1 φ2 x(t);

a first signal generator for generating an oscillator signal f1;

a second signal generator for generating said mono-tonal mixing signal φ2, where the frequency of f1 is a multiple of the frequency of φ2; and

a logic circuit for receiving said oscillator signal f1 and said mono-tonal mixing signal φ2, and generating said multi-tonal mixing signal φ1, where φ1 * φ2 has significant power at the frequency of said local oscillator signal being emulated, neither of said φ1 nor said φ2 having significant power at the carrier frequency of said input signal x(t) or said LO signal being emulated.

2. The circuit of claim 1 wherein said logic circuit comprises an exclusive-OR gate (XOR), and φ1 = f1 XOR φ2.

3. The circuit of claim 1 wherein unwanted power at baseband is minimized by adjusting the frequency of said φ2 signal such that unwanted RF tones do not fall on top of said input signal x(t) at baseband.

4. The circuit of claim 1 wherein unwanted power at baseband is minimized by frequency hopping said φ2 signal so that the probability of unwanted RF tones falling on top of φ1 * φ2 x(t) is significantly reduced.

5. The circuit of claim 1 wherein said first signal generator comprises:

an oscillator for generating an oscillator signal; and

a regenerative divider for receiving said oscillator signal and converting said oscillator signal to said f1 signal.

6. The circuit of claim 5 wherein said oscillator is a voltage-controlled oscillator.

7. The circuit of claim 6 wherein said oscillator that is tuned to a multiple of the carrier frequency of said input signal x(t) and said regenerative divider comprises a divide-by-n element.

8. The circuit of claim 6 wherein said oscillator further comprises a high pass filter.

9. The circuit of claim 1 wherein said first signal generator comprises an oscillator that is tuned to a divisor of the carrier frequency of said input signal x(t) and a multiply-by-n element.

10. The circuit of claim 1 wherein said second signal generator comprises:
a frequency controller; and
a square wave generator.

11. The circuit of claim 10 wherein said second signal generator further comprises:
a divide-by-2 element to ensure that a fifty percent duty cycle is provided.

12. The circuit of claim 10 wherein said frequency controller is operable to hop said $\varphi 2$ signal from one frequency to another, reducing the probability of the output of said circuit having power at an unwanted frequency.

13. The circuit of claim 10 wherein said frequency controller is responsive to noise in said output signal $\varphi 1$ $\varphi 2$ x(t) by adjusting the frequency of $\varphi 2$.

14. The circuit of claim 10 wherein said first mixer comprises an active mixer.

15. The circuit of claim 14 wherein said first mixer comprises an active mixer having adjustable performance.

16. The circuit of claim 15, wherein said active mixer has adjustable gain.

17. The circuit of claim 15, wherein said active mixer has adjustable linearity.

18. The circuit of claim 15, wherein said active mixer comprises a current source whose parameters can be adjusted to control gain and linearity of said active mixer.

19. The circuit of claim 15, wherein said active mixer comprises multiple driver components, each for receiving a different input signal in a multi-standard radio.

20. The circuit of claim 14 further comprising a high pass filter electrically connected between said first mixer and said second mixer.

21. The circuit of claim 20 wherein said second mixer comprises a passive mixer.

22. The circuit of claim 21, wherein each of said active mixer, said high pass filter and said passive mixer is a differential device.

23. The circuit of claim 22, wherein said high pass filter comprises a resistor dividing network for setting the common mode voltage output.

24. The circuit of claim 5 wherein said oscillator, said regenerative divider and said logic circuit are differential.

25. The circuit of claim 24 wherein said logic circuit comprises two exclusive-OR (XOR) gates.

26. The circuit of claim 24 wherein said logic circuit comprises two exclusive-NOR (XNOR) gates.

27. The circuit of claim 24 wherein said logic circuit comprises four AND gates and two OR gates arranged to generate:
$\varphi 1P = (\varphi 2P \text{ AND } f1P) \text{ OR } (\varphi 2N \text{ AND } f1N)$; and
$\varphi 1N = (\varphi 2P \text{ AND } f1N) \text{ OR } (\varphi 2N \text{ AND } f1P)$.

28. The circuit of claim 24 wherein said logic circuit comprises four semiconductor switches arranged to generate:

φ1P = (φ2P AND f1P) OR (φ2N AND f1N); and
φ1N = (φ2P AND f1N) OR (φ2N AND f1P).

29. A method of emulating the demodulation of an input signal x(t) to the product of said input signal with a local oscillator (LO) signal, said method comprising the steps of:

generating an oscillator signal f1;

generating a mixing signal φ2, where f1 is four times the frequency of φ2;

generating an aperiodic mixing signal φ1, using a logic circuit which receives said oscillator signal f1 and said second mixing signal φ2, as inputs, where φ1 * φ2 has significant power at the frequency of a local oscillator signal being emulated, and neither of said φ1 nor said φ2 having significant power at the frequency of said input signal x(t), said LO signal being emulated, or said output signal φ1 φ2 x(t);

mixing said input signal x(t) with said aperiodic mixing signal φ1, to generate an output signal φ1 x(t); and

mixing said signal φ1 x(t) with a second mixing signal φ2, to generate an output signal φ1 φ2 x(t).

30. A computer readable memory medium for storing software code executable to perform the method steps of claim 29.

31. A computer readable memory medium for storing hardware development code to fabricate the device of any one of claims 1 through 28.